push-button dimmer switch

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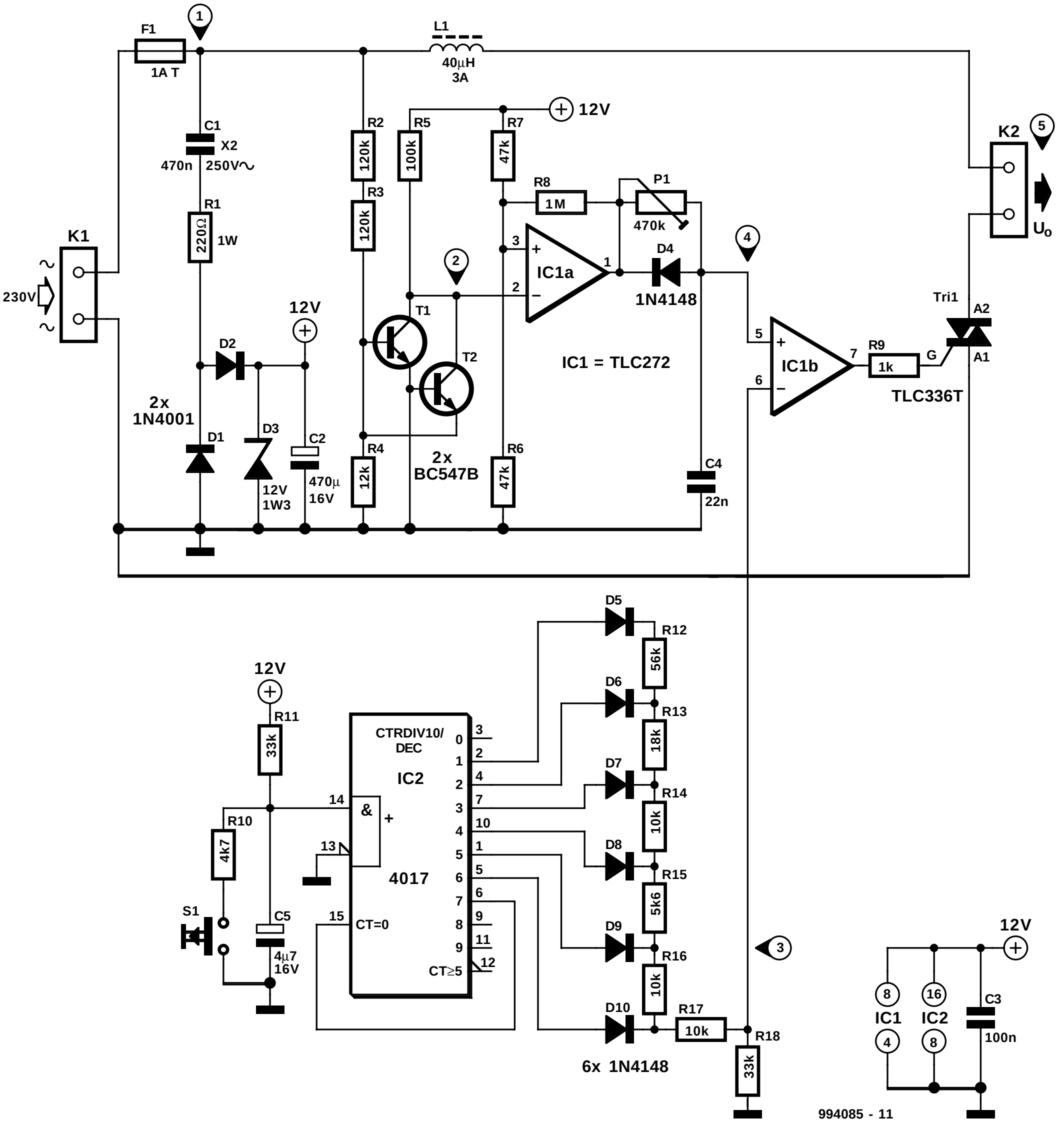

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The present dimmer does not make use of the special integrated circuit for this purpose, the Type SLB0586, but, as the diagram shows, only of standard components. It consists of a power supply, a zero-crossing detector, a comparator with triac for phase gating (phase angle control), and a serial analogue-to-digital converter (ADC).

The power supply section does not use a transformer, but a capacitive potential divider, C_1-R_1-D_1, rectifier D_1-D_2, voltage limiter (to 12 V) D_3, and charging cum decoupling capacitors C_2 and C_3. The 12 V direct voltage is used to power the other sections.

The zero crossings are detected by network R_2–R_5-T_1-T_2. Transistor T_1 is off when the level of the positive half wave of the attenuated mains voltage drops to about 12.6 V, that is, just before the zero crossing. Because of this, the potential at the inverting input of IC_{1a} (test point 2) becomes +12 V, but rapidly returns to its original value when the emitter potential of T_2 becomes negative with respect to earth. This results in short positive pulses around the zero crossing as shown in the timing diagram in Figure 2.

Additionally, the output pulses from IC_{1a} are inverted. Resistors R_6 and R_7 set the threshold potential to 6 V, while resistor R_8 provides some hysteresis. The inverter charges capacitor C_4 via P_1 after each and every zero crossing. During the zero crossings, the output of the inverter briefly goes low, but long enough for C_4 to become discharged rapidly via diode D_4. This results in the sawtooth-like voltage (waveform 4 in Figure 2) at the non-inverting input of comparator IC_{1b}.

The reference voltage for the comparator is provided by counter IC_2. Each time switch S_1 is pressed, the counter progresses one position. After the first time the switch is pressed, Q_1 is active (high), after the second time, Q_2, after the third, Q_3, and so on, until the seventh time when the counter is reset.

Network R_{12}–R_{18}-D_5–D_{10} converts the counter position into an analogue output voltage, U_o:

$$U_o = R_{18}(U_b - U_d)/R,$$

where U_b is the supply voltage, U_d is the diode voltage, and R is the sum of all resistors interconnected by the counter output. The resistors have been selected to ensure floating transition between the various stages. For instance, at the fifth pulse,

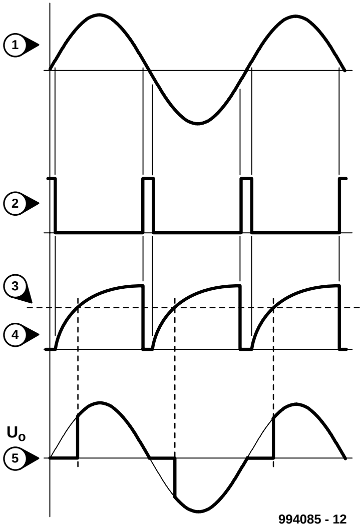
$$U_{o(5)} = R_{18}(U_b - U_d)/(R_{16} + R_{17} + R_{18}) = 7.1\ \text{V},$$

and at the sixth pulse,

$$U_{o(6)} = R_{18}(U_b - U_d)/(R_{17} + R_{18}) = 8.7\ \text{V}.$$

The higher the voltage, the shorter the part of the sawtooth above the threshold that turns on the triac. At $U_{o(6)}$, the output of IC_{1b} is low so that the load remains switched off. At $U_{o(0)}$ (reference voltage), there is no phase gating at all. This may be set with P_1. The phase-gated mains voltage at connector K_2 is shown in the lowest waveform in Figure 2 (U_o).

2



Since there is no isolation of the mains voltage either during use or test, the dimmer must be housed in a well-insulated or plastic enclosure. Switch S_1 must be suitable for carrying mains voltage.

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